

Multicore Computer Architecture - Storage and Interconnects

Tutorial 6

Concepts in TCMP systems



NPTEL Online Course : Multi-Core Computer Architecture - Storage and Interconnects, Dr. John Jose, IIT Guwahati

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Tutorial Problem-1

- ❖ Consider a multicore system with a 4x4 mesh NoC where each core consists of a processing element a private L1 cache and a shared distributed L2 cache. Each core has a private L1-I cache and a private L1-D cache, each of which is 8KB and are using direct mapping. The total L2 cache on the chip is 1MB and L2 uses 16B block and is 16 way associative. Each L2 cache on chip has all the 16 ways of the sets assigned to it. The L2 cache memory per core division is such that total sets in L2 cache are uniformly divided into all the cores in sequential fashion. Cache miss request packet generation and cache miss reply packet generation take 2 cycles each at the respective cores. Assume a cache block can be contained in a single flit. The NoC uses single flit packets. The system uses a 32 bit physical address. Consider a 2 cycle router and 1 cycle link for the NoC that uses XY routing. Two cores – P4 and P12 generated L1 cache misses on the physical addresses 0x 34127568 and 0x 4A2329A1 respectively. All these misses were hits in respective L2 caches. Find the miss penalties at zero load in network.

Tutorial Problem-1

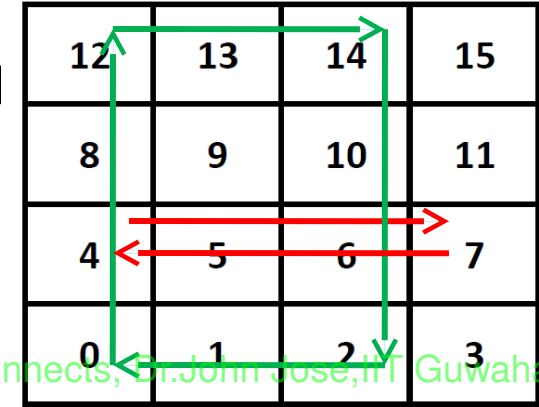
- ❖ Consider a multicore system with a 4x4 mesh NoC where each core consists of a processing element a private L1 cache and a shared distributed L2 cache. Each core has a private L1-I cache and a private L1-D cache, each of which is 8KB and are using direct mapping. The total L2 cache on the chip is 1MB and L2 uses 16B block and is 16 way associative. Each L2 cache on chip has all the 16 ways of the sets assigned to it. The L2 cache memory per core division is such that total sets in L2 cache are uniformly divided into all the cores in sequential fashion. Cache miss request packet generation and cache miss reply packet generation take 2 cycles each at the respective cores. Assume a cache block can be contained in a single flit. The NoC uses single flit packets. The system uses a 32 bit physical address. Consider a 2 cycle router and 1 cycle link for the NoC that uses XY routing. Two cores – P4 and P12 generated L1 cache misses on the physical addresses 0x 34127568 and 0x 4A2329A1 respectively. All these misses were hits in respective L2 caches. Find the miss penalties at zero load in network.

Tutorial Problem-1

❖ Two cores – P4 and P12 generated L1 cache misses on the physical addresses 0x 34127568 and 0x 4A2329A1 respectively

❖ Total L2- cache 1MB, 16B block, 16 way

❖ #sets = 2^{12} 12 bits index.



Tag=16

Index=12

Offset=4

Tile=4

Set=8

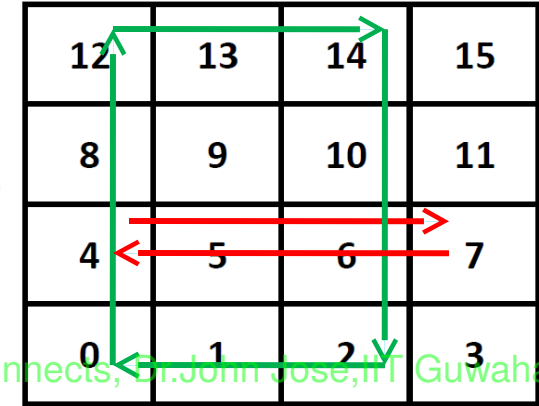
❖ P4 -> 0x 34127568: 0111 0101 0110 1000 Tile = 7

❖ P12-> 0x 4A2329A1: 0010 1001 1010 0001 Tile = 2

Tutorial Problem-1

❖ P4 -> 0x 34127568: 0111 0101 0110 1000 Tile = 7

Req. create	hop	eject	Reply create	hop	eject	total
2	3x3=9 4.5.6.7	2	2	3x3=9 7.6.5.4	2	26



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❖ P12-> 0x 4A2329A1: 0010 1001 1010 0001 Tile = 2

Req. create	hop	eject	Reply create	hop	eject	total
2	5x3=15 12>13>14 >10>6>2	2	2	5x3=15 2>1>0>4 >8>12	2	38

Tutorial Problem-2

- ❖ Consider a TCMP system with a 8x8 mesh NoC where each tile consists of a superscalar processor a private L1 cache and a shared distributed L2 cache. Let $T_0, T_1, T_2, \dots, T_{63}$ corresponds to the tiles. The total L2 cache on the chip is 16MB and L2 uses 64B block and is 16-way associative. Each L2 cache on chip has all the 16 ways of the sets assigned to it. The L2 cache memory per tile division is such that total sets in L2 cache are uniformly partitioned across all tiles in sequential fashion. The system uses a 32-bit physical address. Tile T_{12} generated a cache misses for the address 0x34120568 and tile T_3 generated an L1 cache miss on the address 0xA02359A0. Where are these addresses mapped in TCMP?

Tutorial Problem-2

- ❖ Consider a TCMP system with a **8x8 mesh NoC** where each tile consists of a superscalar processor a private L1 cache and a shared distributed L2 cache. Let T0, T1, T2... ,T63 corresponds to the tiles. The total L2 cache on the chip is **16MB** and L2 uses **64B block** and is **16-way associative**. Each L2 cache on chip has all the 16 ways of the sets assigned to it. The L2 cache memory per tile division is such that total sets in L2 cache are uniformly partitioned across all tiles in sequential fashion. The system uses a **32-bit physical address**. Tile **T52** generated a cache misses for the address **0x34120568** and tile **T3** generated an L1 cache miss on the address **0xA02359A0**. Where are these addresses mapped in TCMP?
- ❖ Total L2- cache 16 MB, 64B block, 16 way
- ❖ #sets = 2^{14} 14 bits index.

Tag=12

Index=14

Offset=6

Tile=6

Set=8

Tutorial Problem-2

- ❖ The system uses a 32-bit physical address. Tile T52 generated a cache misses for the address 0x34120568 and tile T3 generated an L1 cache miss on the address 0xA02359A0.

Tag=12

Index=14

Offset=6

Tile=6

Set=8

- ❖ Total L2- cache 16 MB, 64B block, 16 way

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- ❖ #sets = 2^{14} 14 bits index.

- ❖ 0x34120568 0x34120568

- ❖ 0010 0000 0101 0110 1000

- ❖ 0010 0000 0101 0110 1000

- ❖ Tile 8 (T8) : Packet from T52 to T8

56	57	58	59	60	61	62	63
48	49	50	51	52	53	54	55
40	41	42	43	44	45	46	47
32	33	34	35	36	37	38	39
24	25	26	27	28	29	30	31
16	17	18	19	20	21	22	23
8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7

Tutorial Problem-2

- ❖ The system uses a 32-bit physical address. Tile T52 generated a cache misses for the address 0x34120568 and tile **T3 generated an L1 cache miss on the address 0xA02359A0.**

Tag=12

Index=14

Offset=6

Tile=6

Set=8

- ❖ Total L2- cache 16 MB, 64B block, 16 way

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- ❖ #sets = 2^{14} ✉ 14 bits index.

- ❖ 0xA02359A0 ✉ 0xA0**2359**A0

- ❖ 0011 0101 1001 1010 0000

- ❖ 0011 0101 1001 1010 0000

- ❖ Tile 13 (T13) : Packet from T3 to T13

56	57	58	59	60	61	62	63
48	49	50	51	52	53	54	55
40	41	42	43	44	45	46	47
32	33	34	35	36	37	38	39
24	25	26	27	28	29	30	31
16	17	18	19	20	21	22	23
8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7

**THANK
YOU!**

FOR

YOUR

PRESENCE

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